

**Low Power Circuits with Small Voltage Swing Transmission, Voltage Regeneration,
and Wide Bandwidth Architecture**

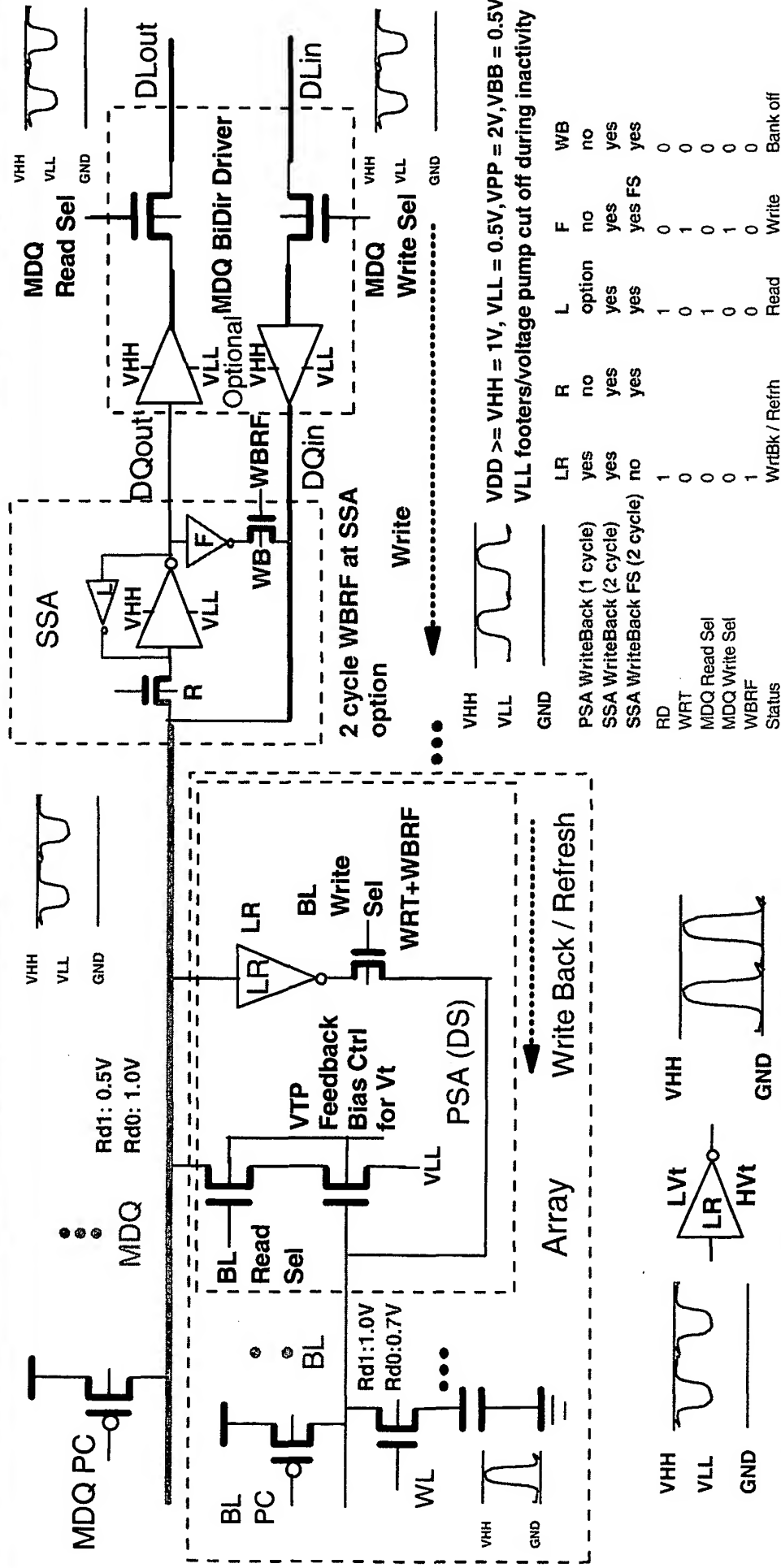
APPENDIX

5 Eleven figures are attached as appendix pages A2 to A12, schematically showing examples of embodiments of the invention.

[illegible]

Figure shows separate datelines for Read and Write. They can be combined as bi-directional datelines for both Read and Write.

Low Power Hierarchical Direct Sensing w/ Local Write Back



P LVt and N HVt devices well bias generated via VTP feedback



Read, Write, WriteBack Control Table

	LR	R	L	F	WB
PSA WriteBack (1 cycle)	yes	no	option	no	no
SSA WriteBack (2 cycle)	yes	yes	yes	yes	yes
SSA WriteBack FS (2 cycle)	no	yes	yes	yes FS	yes
RD	1	1	0	0	
WRT	0	0	1	0	
MDQ Read Sel	0	1	0	0	
MDQ Write Sel	0	0	1	0	
WBRF	1	0	0	0	
Status	WrtBk / Refrh	Read	Write	Bank off	

1. WriteBack can be local at PSA or at remote SSA

2. Write Data can be small swing or full swing on MDQ

3. Local WriteBack (smaller power), remote WriteBack (smaller area)

4. Local WriteBack writes better to cells

5. One cycle or two cycle writeback option

Read cycle, Write cycle = 3 ns

Read + Write Back cycle = 4.5 ns < Read cycle + Write cycle (6 ns)

The above is the control table for the various operations: READ, WRITE, WRITEBACK REFRESH. For READ operation, RD and MDQ_READ_SEL are HIGH. For WRITE operation, WRT and MDQ_WRITE_SEL are HIGH. For WRITEBACK REFRESH operation, RD and WBRF are HIGH.

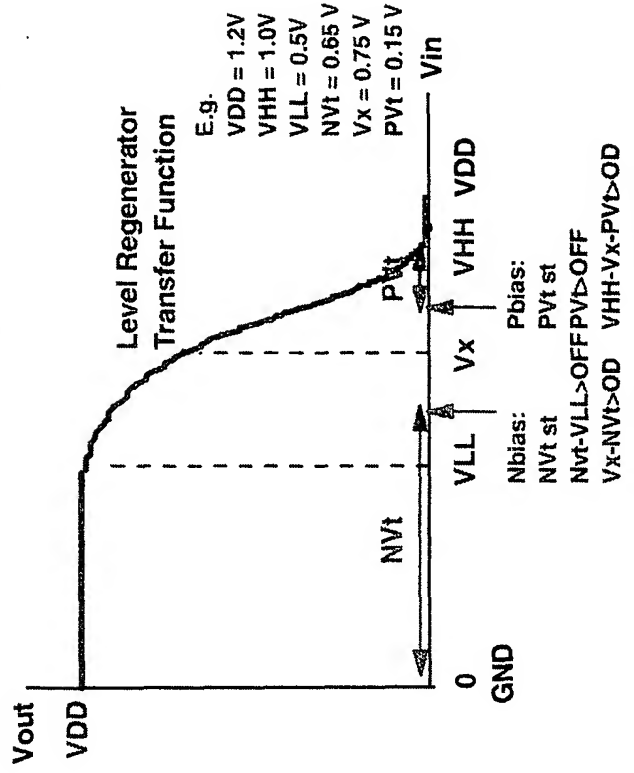
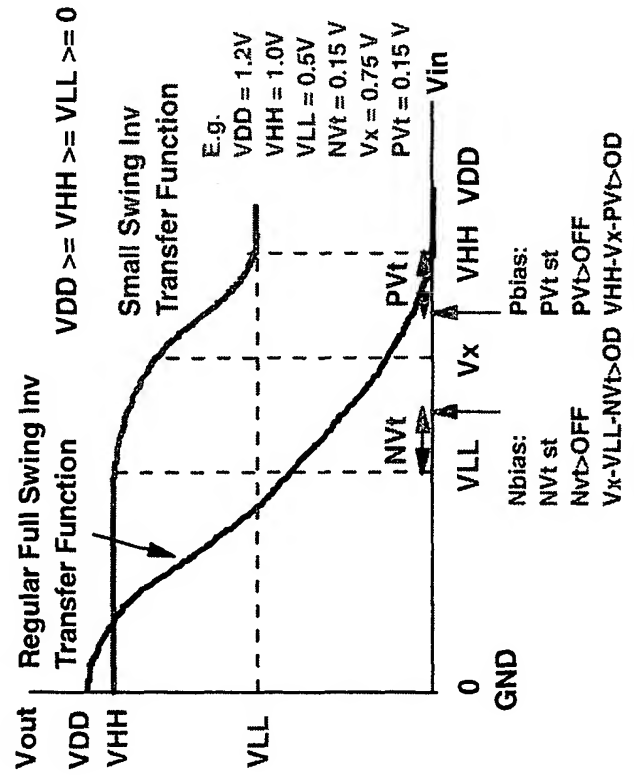
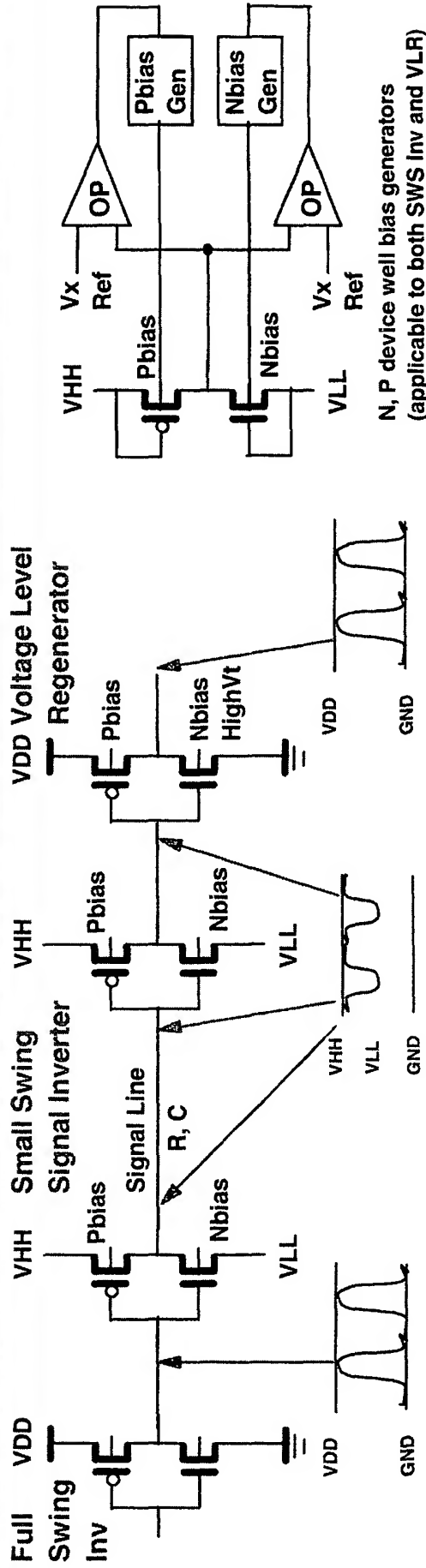
Since DRAM cell voltage is "destroyed" after each READ operation (due to charge sharing), WRITEBACK is an operation to restore the DRAM cell voltage (logic data) after a READ.

For PSA (primary sense amplifier) to perform a WRITEBACK, the level restoring logic LR is used, as shown in the above table.

WRITEBACK can be performed from the SSA, by using the level restoring logic LR, the READ mux (R), the SSA latch (L), the SSA feedback logic (F) and the SSA WRITEBACK mux (WB), as shown in the above table.

The traditional full swing WRITEBACK can be performed from the SSA, without the level restoring logic (LR) in the PSA, the READ mux (R), the SSA latch (L), the SSA feedback logic (F) operated in full swing mode, and the SSA WRITEBACK mux (WB), as shown in the above table.

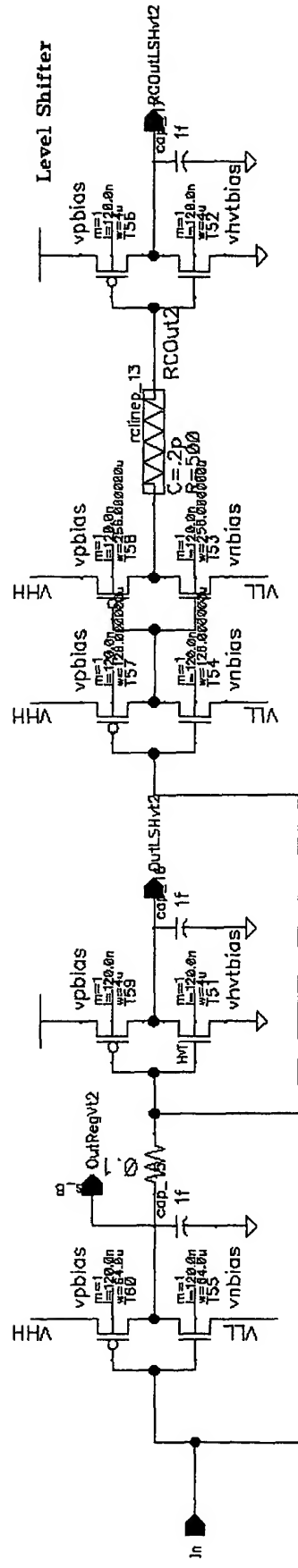
Small Swing Signal Inverter, Level Regenerator and Bias Generator



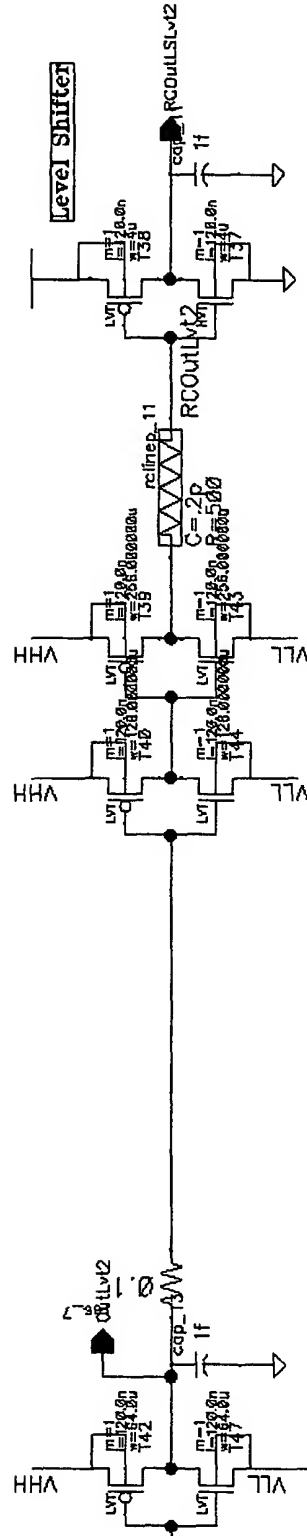
N, P device well bias of Small Swing Inv is generated via VTP feedback

N, P device well bias of L v I R gen rator is g n rated via VTP feedback

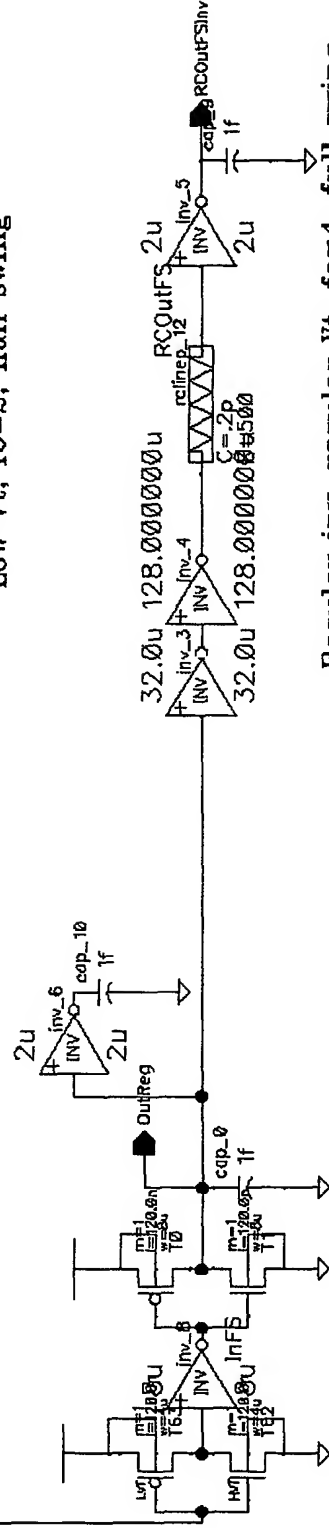
Small Voltage Swing Data Transmission and Regeneration



Regular Vt with forward bias, fo=2, half swing



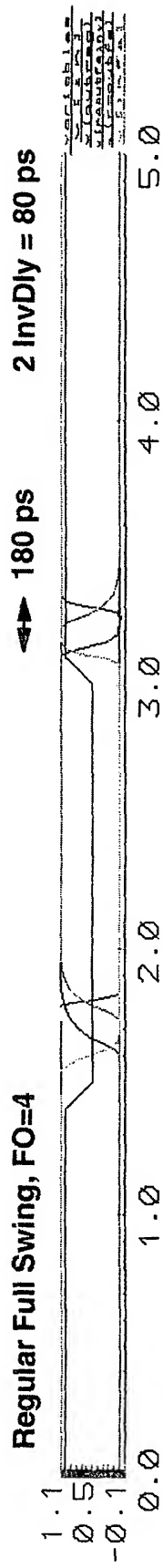
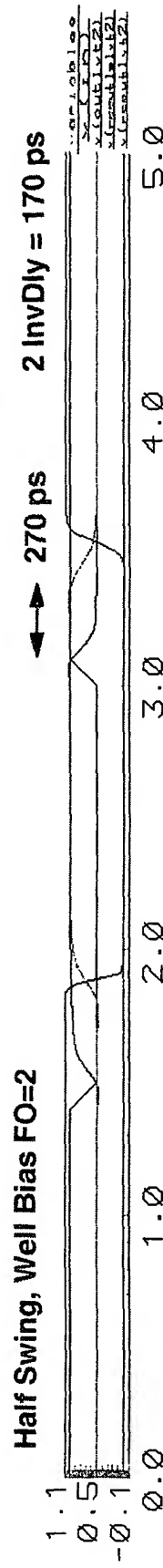
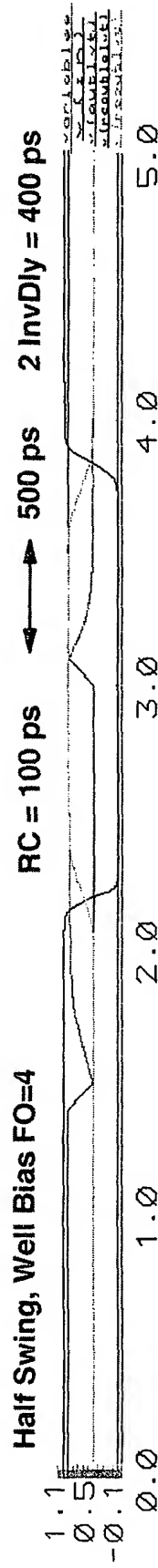
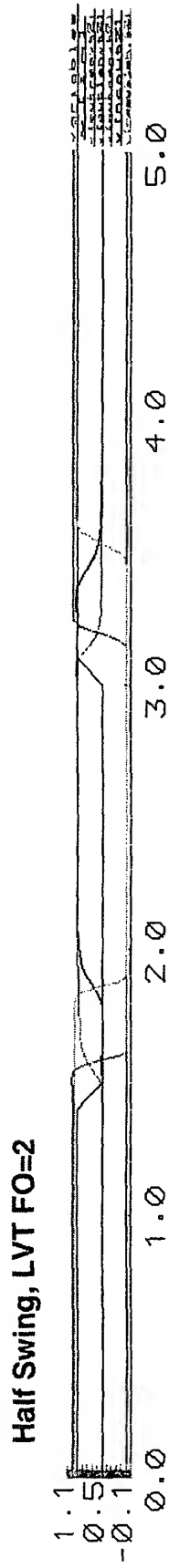
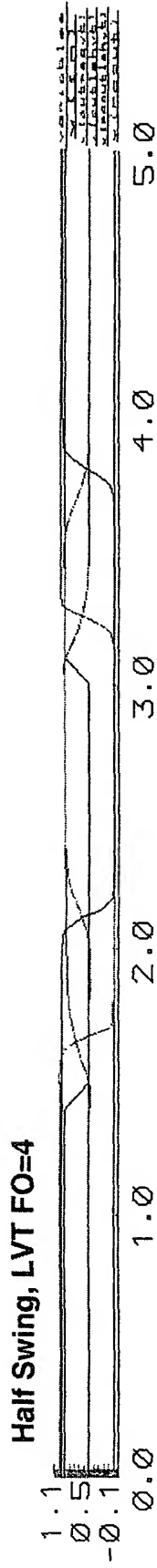
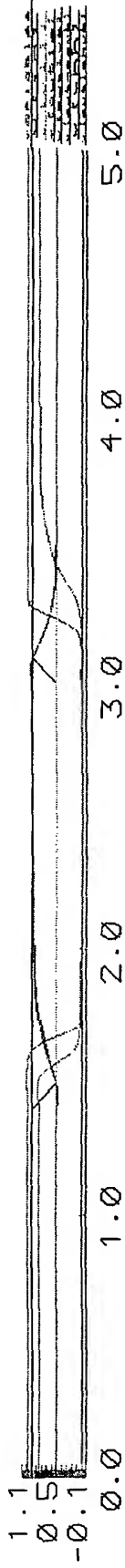
Low Vt, fo=2, half swing



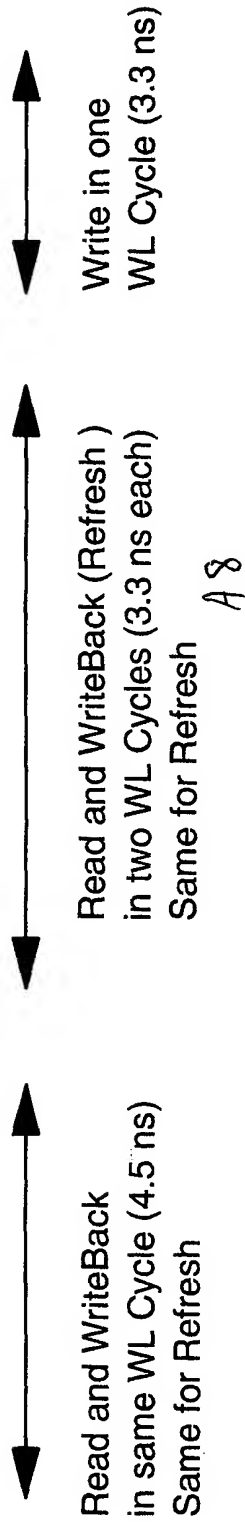
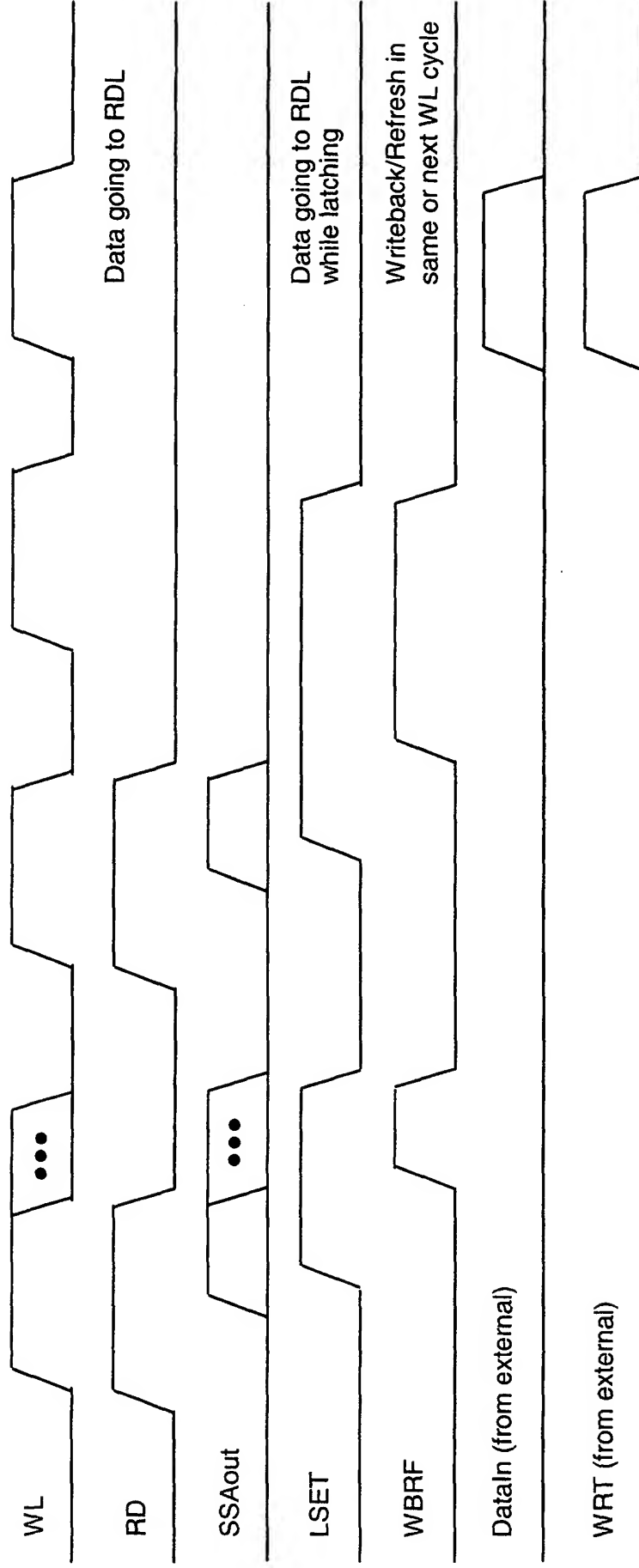
Regular inv, regular Vt, fo=4, full swing

Small Voltage Swing Data Transmission and Regeneration

*BIN: ----



Different Mode of Read, Write and WriteBack/Refresh

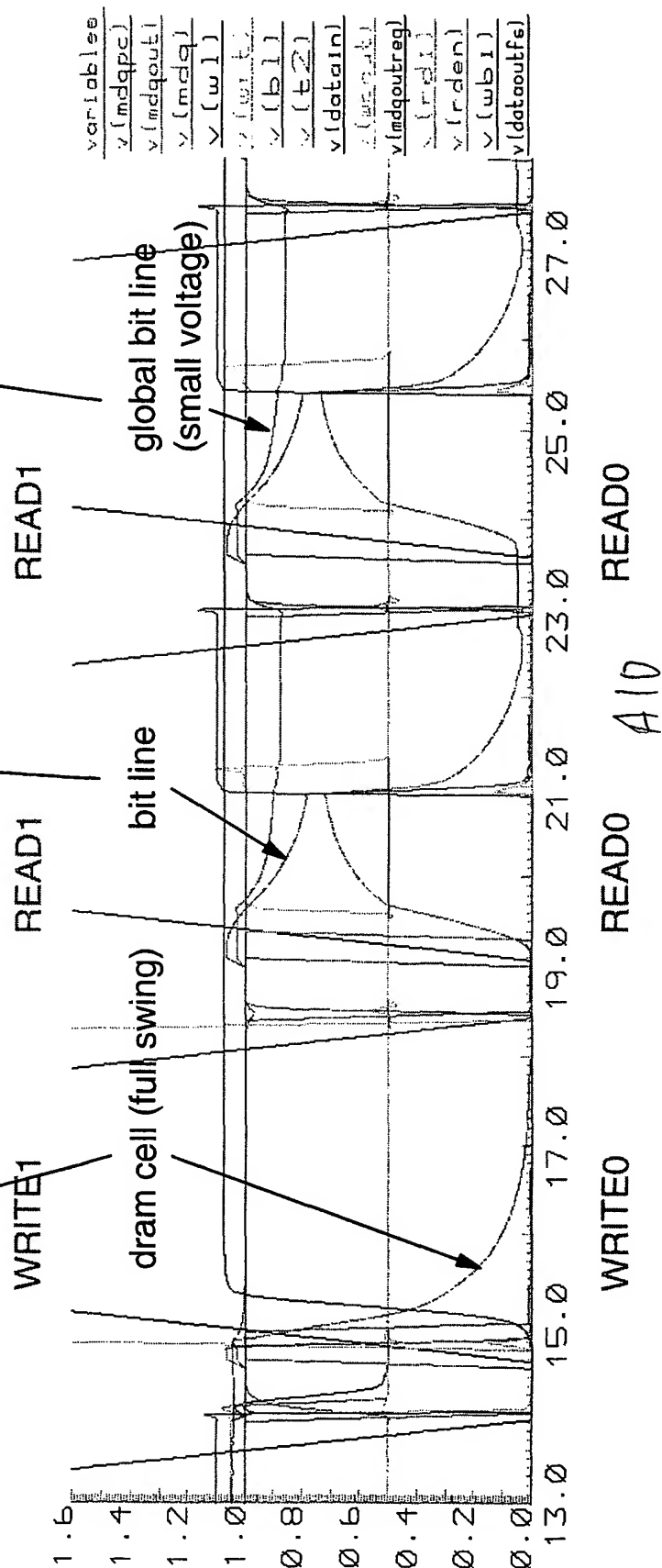
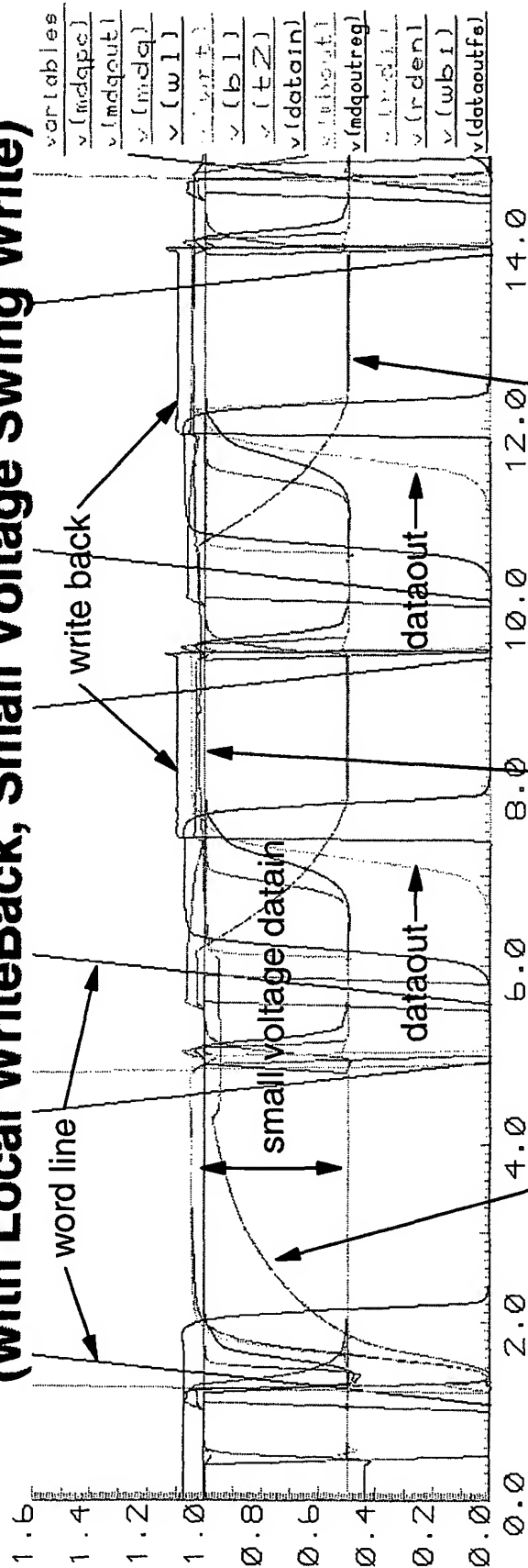


HHH
VLL
vbb
vbias
vbias
vbbias



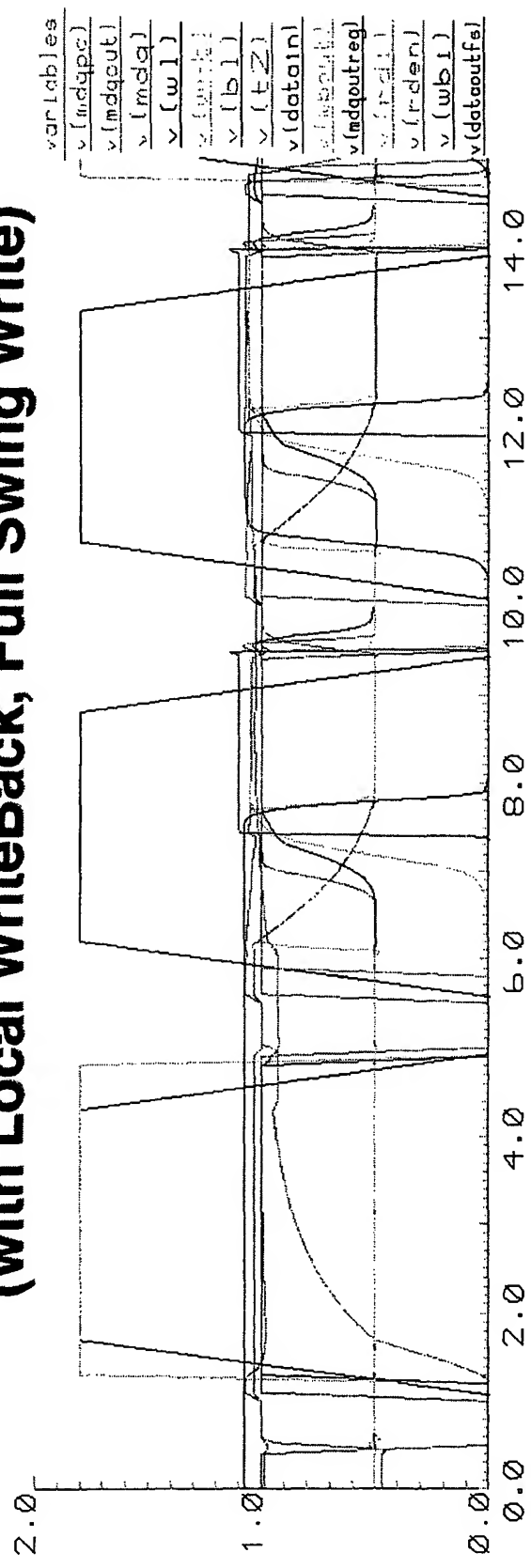
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Small Voltage Swing Hierarchical Direct Sensing (with Local WriteBack, Small Voltage Swing Write)

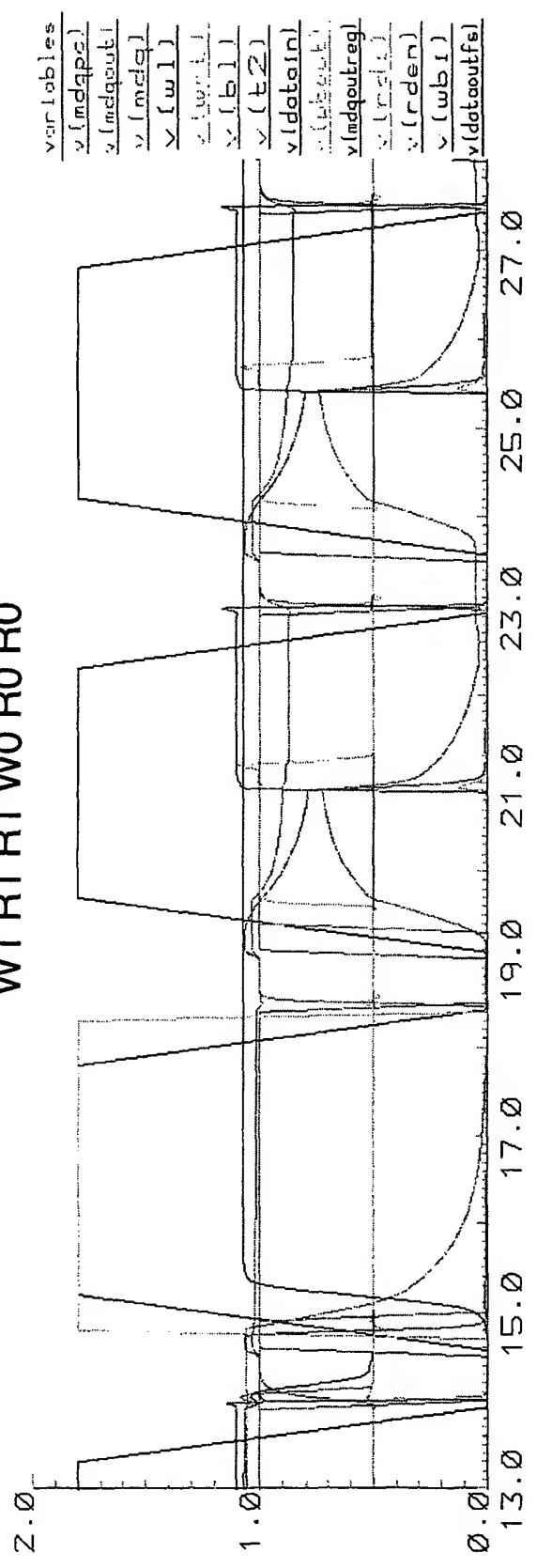


Small Voltage Swing Hierarchical Direct Sensing (with Local WriteBack, Full Swing Write)

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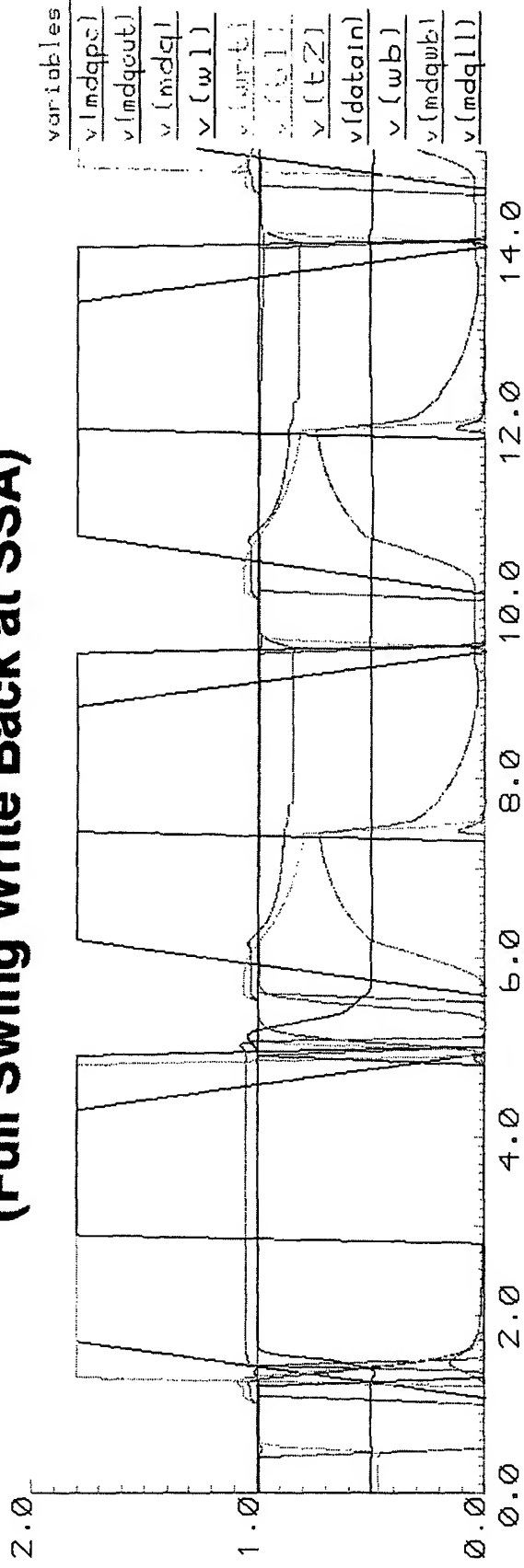
W1 R1 R1 W0 R0 R0



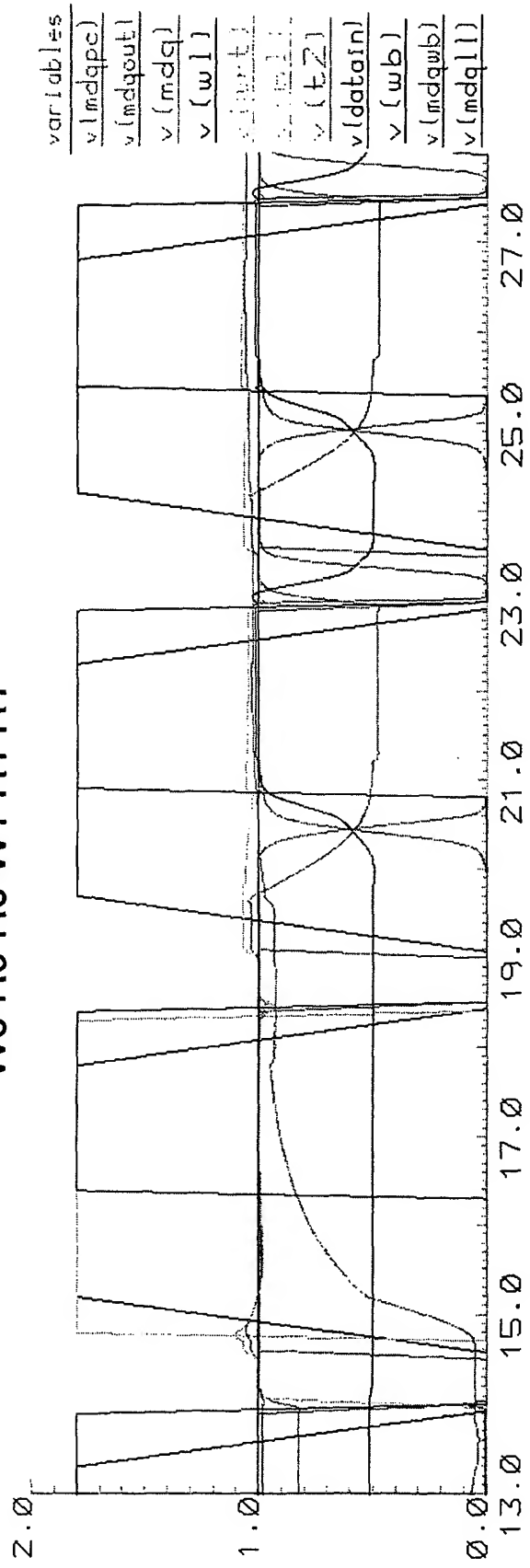
A 11

*BIN: ----

Small Voltage Swing Hierarchical Direct Sensing (Full Swing Write Back at SSA)



W0 R0 R0 W1 R1 R1



A12